## Amendments to the Specification

Please replace the Title of the Invention with the following new Title:

SEMICONDUCTOR MEMORY DEVICE WITH REDUCED MEMORY CELL AREA

Please amend the paragraph beginning on page 2, line 21, as follows:

A semiconductor memory device according to the present invention includes a memory cell, an interlayer insulation film and a capacitive element. The memory cell is formed on a semiconductor substrate, and has a pair of inverters each including a driver MOS (Metal Oxide Semiconductor) transistor and a load element, and an access MOS transistor. The interlayer insulation film covers the access MOS transistor, the driver MOS transistor and the load element. The capacitive element is formed on the interlayer insulation film, and electrically connected to drain of the access MOS transistor, drain of the driver MOS transistor, and the load element. The gate width of the driver MOS transistor is at ~~least~~ most 1.2 times longer than the gate width of the access MOS transistor.

Please amend the paragraph beginning on page 7, line 1, as follows:

In the present embodiment, in an attempt to have an access transistor and a driver transistor of approximately the same size as described above, a capacitive element of about ~~10pF-30pF~~ 10fF-30fF is connected to a memory node, or the resistance value at a contact part of access transistor and/or driver transistor and another element is appropriately adjusted. Specifically, for example, the resistance value at the contact part of an access transistor and a bit

line is set to about 21-100kΩ, for example, while the resistance value of the contact part of a driver transistor and a ground line (GND line) is set to about 20kΩ at most, for example, thus setting the resistance value of the contact part of the access transistor and the bit line larger than the other one.

Please amend the paragraph beginning on page 8, line 16, as follows:

Then the potential difference occurs between the source and the drain of second driver nMOS transistor 4, discharging the charges to GND line. The bit line capacitance, source-drain current value of an access transistor, the capacitance of a capacitive element, the source-drain current value of a driver transistor are set such that the potential of second memory node 10 at this time does not exceed the inverted threshold value of the inverter including first [[TRT]] TFT 7 and first driver nMOS transistor 3, which has second memory node 10 as an input.

Please amend the paragraph beginning on page 10, line 7, as follows:

Next, conditions when non-destructive reading is performed will be described, in which a data in a memory cell is not destructed during a reading operation. Referring to Fig. 15, the dependency of the maximum potential of a memory [[mode]] node on the capacitance value of a capacitor during a reading operation will be described. The ordinate and the abscissa indicate the capacitance value of a capacitor and the maximum potential of a memory node.

Please amend the paragraphs beginning on page 16, line 7, as follows:

As shown in Fig. 3, in a layer above first inter connection patterns 20-22 and active region patterns 23, 24, first contact hole patterns (contact parts) 26-31 and second contact hole patterns (contact parts) 32, [[22]] 33 are formed.

First contact hole patterns 26, 27 are the patterns of contact holes each connecting the source of driver nMOS transistor and an upper layer interconnection, first contact hole patterns 28, 29 are the patterns of contact holes each connecting active region corresponding to a memory node and an upper layer interconnection, first contact hole patterns 30, 31 are the patterns of contact holes each connecting an access MOS transistor and a bit line, and second contact hole patterns 32, [[22]] 33 are the patterns of contact holes each connecting the gate of driver nMOS transistor and an upper layer interconnection.

Please amend the paragraph beginning on page 16, line 27, as follows:

As shown in Fig. 4, in a layer above first ~~inter-connection~~ contact hole patterns 26-31 and second contact hole patterns 32, [[22]] 33, second ~~contact hole~~ interconnection patterns ~~(contact parts)~~ 38-41, third contact hole patterns (contact parts) 34-37 and fourth contact hole patterns (contact parts) 42-45 are formed.

Please amend the paragraph beginning on page 20, line 1, as follows:

An example of capacitive element patterns 52, 53 may be a cylindrical capacitor. In the example shown in Fig. [[4]] 6, the two-dimensional shape of capacitance element patterns 52, 53 are quadrangular, but it may be any other form such as circle, triangle, square, polygon with five and more corners. Capacitor element patterns 52, 53 each have the lower electrode (first

electrode), the capacitor insulation film (dielectric film) and the upper electrode (second electrode) as described above.